WHAT IS CLAIMED

1. A control circuit for a switch mode DC-DC converter comprising an arrangement of monitored LGATE, UGATE and PHASE node condition threshold detectors, outputs of which are processed in accordance with a switching control operator to ensure that each of an upper FET (UFET) and a lower FET (LFET) is completely turned off before the other FET begins conduction, thereby maintaining a dead time that exhibits no shoot-through current and is independent of the type of switching FET.

2. The control circuit according to claim 1, wherein, subsequent to turn off of the LFET, and in response to the voltage at the PHASE node having reached a prescribed negative polarity voltage following a blanking delay, said switching control operator is operative to trigger turn-on of the UFET, which causes the phase node voltage to go high.

3. The control circuit according to claim 2, wherein, in the absence of said PHASE node having reached said prescribed negative polarity voltage subsequent to the LGATE voltage going low, and in response to said PHASE node having reached prescribed positive threshold following a blanking delay, said switching control operator is operative to trigger turn-on of the UFET, which causes the phase node voltage to go high.

4. The control circuit according to claim 3, wherein, in response to the elapse of a prescribed time-out without either of prescribed positive and negative polarity thresholds having been reached at said phase node following a blanking delay, said switching control operator is operative to trigger turn-on of the UFET, so that the voltage at the phase node goes high.

5. The control circuit according to claim 1, wherein, subsequent to turn-off of said UFET, and in response to the UGATE voltage dropping to a voltage level that is a prescribed value above the phase voltage, said switching control operator is operative to trigger a prescribed time out before turning on said LFET.

6. The control circuit according to claim 5, wherein, subsequent to turn-off of said UFET, and in response to the level of the PHASE node voltage reaching a predetermined threshold voltage, said switching control operator is operative to turn on said LFET.

7. A method for controlling a switch mode DC-DC converter having an upper FET (UFET) and a lower FET (LFET) coupled between power supply voltage rails, and having a common phase node therebetween, said method comprising the steps of:

(a) monitoring LGATE, UGATE and PHASE node voltages; and

(b) subsequent to turn off of said LFET, and in response to the voltage at the PHASE node having reached a prescribed negative polarity voltage following a blanking delay, triggering turn-on of the UFET, so as to cause said phase node voltage to go high.

8. The method according to claim 7, wherein step (b) further comprises, in the absence of said PHASE node having reached said prescribed negative polarity voltage subsequent to the LGATE voltage going low, and in response to said PHASE node having reached prescribed positive threshold following a blanking delay, triggering turn-on of said UFET, so as to cause said phase node voltage to go high.

9. The method circuit according to claim 8, wherein step (b) further comprises, in response to the elapse of a prescribed time-out without either of prescribed positive and negative polarity thresholds having been reached at said phase node following a blanking delay, triggering turn-on of said UFET, so that the voltage at said phase node goes high.

10. A method for controlling a switch mode DC-DC converter having an upper FET (UFET) and a lower FET (LFET) coupled between power supply voltage rails, and

having a common phase node therebetween, said method comprising the steps of:

(a) monitoring LGATE, UGATE and PHASE node voltages; and

(b) subsequent to turn-off of said UFET, and in response to the UGATE voltage dropping to a voltage level that is a prescribed value above the phase voltage, triggering a prescribed time out and then turning on said LFET.

11. A method for controlling a switch mode DC-DC converter having an upper FET (UFET) and a lower FET (LFET) coupled between power supply voltage rails, and having a common phase node therebetween, said method comprising the steps of:

(a) monitoring LGATE, UGATE and PHASE node voltages; and

(b) subsequent to turn-off of said UFET, and in response to the level of the PHASE node voltage reaching a predetermined threshold voltage, turning on said LFET.